We claim:

1. A semiconductor structure for storing charges, comprising:

an insulator layer having a first compound that includes substances; and

a conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer.

2. The semiconductor structure of claim 1, wherein the first compound includes ditantalum pentaoxide.

3. The semiconductor structure of claim 1, wherein the first substance includes ruthenium atoms.

4. The semiconductor structure of claim 1, wherein the second substance includes oxygen atoms.

5. The semiconductor structure of claim 1, wherein the second compound includes RuO_x, wherein x is indicative of a desired number of atoms.

6. A semiconductor structure for storing charges, comprising:

an insulator layer; and

a conductive layer having a compound formed from a first substance and a second substance, wherein the conductive layer includes a trace amount of the first substance, wherein the morphology of the semiconductor structure remains stable when the trace amount of the first substance is oxidized during crystallization of the insulator layer.

7. The semiconductor structure of claim 6, wherein the compound includes RuO_x, wherein x is indicative of a desired number of atoms.

8. The semiconductor structure of claim 6, wherein the first substance includes ruthenium.

9. The semiconductor structure of claim 6, wherein the second substance includes oxygen.

10. The semiconductor structure of claim 6, wherein the insulator layer includes ditantalum pentaoxide.

Subt B3

11. A semiconductor structure for storing charges, comprising:

an insulator layer having a permittivity value greater than about 25; and

a conductive layer having a compound, wherein the compound remains stable when the insulator layer is crystallized at a high temperature so as to decrease the charge leakage of the insulator layer.

12. The semiconductor structure of claim 11, wherein the insulator layer includes ditantalum pentaoxide.

13. The semiconductor structure of claim 11, wherein the compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

14. The semiconductor structure of claim 11, wherein the high temperature includes greater than about 750 degrees Celsius to less than about 801 degrees Celsius.

15. The semiconductor structure of claim 11, wherein the conductive layer passivates the insulator layer from undesired oxidation.

Subt B4

16. A semiconductor structure for storing charges, comprising:

an insulator layer having a permittivity value; and

a conductive layer abuttingly coupled to the insulator layer, wherein the crystalline structure of the insulator layer describes a desired lattice plane such that the permittivity value of the insulator layer is greater than about 25.

17. The semiconductor structure of claim 16, wherein the insulator layer includes ditantalum pentaoxide.

18. The semiconductor structure of claim 16, wherein the conductive layer includes RuO_x, wherein the x indicates a desired number of atoms.

19. The semiconductor structure of claim 16, wherein the desired lattice plane includes substantially a (001) plane.

20. The semiconductor structure of claim 16, wherein the desired lattice plane is described by three axes, wherein the desired lattice plane is parallel to two of the three axes and intersects one of the three axes.

21. A capacitor comprising:

a first electrode;

a dielectric that includes ditantalum pentaoxide; and

a second electrode having a compound that includes a first substance and a

second substance, wherein the compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion at a high temperature, wherein the compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

22. A capacitor comprising:

a first electrode;

a dielectric that includes ditantalum pentaoxide; and

a second electrode having a compound that includes a first substance and a second substance, wherein the second electrode includes a trace amount of the first substance, wherein the morphology of the semiconductor structure remains stable when the trace amount of the first substance is oxidized during crystallization of the dielectric, wherein the compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

23. A capacitor comprising:

a first electrode;

a dielectric that includes ditantalum pentaoxide; and

a second electrode having a compound, wherein the crystalline structure of the dielectric describes a (001) lattice plane, wherein the compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

24. A capacitor comprising:

a first electrode;

a dielectric having a first compound that includes a first substance and a second substance, wherein the first compound includes ditantalum pentaoxide; and

a second electrode having a second compound that includes a third substance and a fourth substance, wherein the second electrode includes a trace amount of the third substance, wherein the second compound in an as-deposited state includes a substantial amount of the fourth substance, wherein the trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion of at least one of the first substance and the second substance is inhibited, wherein the crystalline structure of the dielectric describes substantially a (001) lattice plane, and wherein the second compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

25. A capacitor comprising:

a first electrode having a substance that is selected from a group consisting of TiN, TiON, WN_x, TaN, Ta, Pt, Pt-Rh, Pt-RhO_x, Ru, RuO_x, Ir, IrO_x, Pt-Ru, Pt-RuO_x, Pt-Ir, Pt-IrO_x, $SrRuO_3$, Au, Pd, Al, Mo, Ag, and Poly-Si;

a dielectric having a first compound that includes a first substance and a second substance, wherein the first compound includes ditantalum pentaoxide; and

a second electrode having a second compound that includes a third substance

and a fourth substance, wherein the second electrode includes a trace amount of the third substance, wherein the second compound in an as-deposited state includes a substantial amount of the fourth substance, wherein the trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion of at least one of the first substance and the second substance is inhibited, wherein the crystalline structure of the dielectric describes substantially a (001) lattice plane, and wherein the second compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

26. A method for enhancing a dielectric, comprising:

forming an as-deposited film of a conductive compound that includes a first substance and a second substance, wherein the act of forming incorporates a substantial amount of the second substance in the as-deposited film so as to inhibit undesired oxidation of the first substance at a high temperature; and

forming the dielectric over the conductive compound.

27. The method of claim 26, wherein the first substance includes ruthenium.

28. The method of claim 26, wherein the second substance includes oxygen.

29. The method of claim 26, wherein the conductive compound includes RuO_x,

wherein the x is indicative of a desired number of atoms.

30. The method of claim 26, wherein the dielectric includes ditantalum pentaoxide.

31. A method for enhancing a semiconductor structure that stores charges, comprising:

forming an as-deposited film of a conductive compound that includes a first substance and a substantial amount of a second substance so as to inhibit volatile oxide states caused by the first substance; and

forming the dielectric over the conductive compound.

32. The method of claim 31, wherein forming includes forming in about 210 degrees Celsius.

33. The method of claim 31, wherein forming includes forming with a first substance, wherein the first substance includes about 200 sccm of Ru-HEC.

34. The method of claim 31, wherein forming includes forming with a second substance, wherein the second substance includes about 250 sccm of O_2.

35. The method of claim 31, wherein forming includes forming at a pressure of about 2.5 torrs.

36. A method for enhancing a semiconductor structure that stores charges, comprising:

forming an as-deposited film of ruthenium oxide that includes a substantial amount of oxygen so as to inhibit morphological change caused by oxidation of ruthenium;

crystallizing the as-deposited film to form a crystallized film; and

forming the dielectric over the crystallized film.

37. The method of claim 36, wherein crystallizing includes crystallizing at a temperature that is greater than about 750 degrees Celsius and less than about 800 degrees Celsius.

38. The method of claim 36, wherein crystallizing includes crystallizing in an ambient of nitrogen.

39. The method of claim 36, wherein the act of crystallizing results in compounds and substances that include ruthenium dioxide and a trace amount of ruthenium.

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40. The method of claim 36, wherein forming the as-deposited film depositing the as-deposited film using a technique of chemical vapor deposition.

41. A method for enhancing a semiconductor structure that stores charges, comprising:

forming a conductive layer of RuO_x;

crystallizing to form RuO_2 and a trace amount of Ru;

forming an amorphous insulator layer of Ta_2O_5; and

crystallizing to form crystallized Ta_2O_5, wherein the act of crystallizing to form crystallized Ta_2O_5 converts the trace amount of Ru into RuO_2.

42. The method of claim 41, wherein crystallizing to form crystallized Ta_2O_5 includes crystallizing at a temperature of about 800 degrees Celsius.

43. The method of claim 41, wherein crystallizing to form crystallized Ta_2O_5 includes crystallizing in an ambient of dinitrogen oxide.

44. The method of claim 41, wherein crystallizing to form crystallized Ta_2O_5 includes crystallizing in an ambient of oxygen.

45. The method of claim 41, wherein crystallizing to form crystallized Ta_2O_5 acts to passivate the conductive layer from volatility caused by the trace amount of Ru.

46. A method for enhancing a semiconductor structure that stores charges, comprising:

forming a conductive layer of RuO_x;

crystallizing to form RuO_2 and a trace amount of Ru;

forming an amorphous insulator layer of Ta_2O_5; and

forming a crystallized Ta_2O_5 with a desired lattice plane such that the permittivity of the crystallized Ta_2O_5 is greater than about 25.

47. The method of claim 46, wherein forming a crystallized Ta_2O_5 includes forming substantially a (001) lattice plane.

48. The method of claim 46, wherein forming a conductive layer of RuO_x includes forming with a substantial amount of oxygen.

49. The method of claim 46, wherein crystallizing includes crystallizing at a temperature of greater than about 750 degrees Celsius to less than about 800 degrees Celsius.

50. The method of claim 46, wherein forming a crystallized Ta_2O_5 includes forming at a temperature of about 800 degrees Celsius.

51. A memory device comprising:

an array of memory cells, wherein the array includes at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer;

an address decoder;

a row access circuitry;

a column access circuitry;

a controller; and

an input/output circuit.

52. An electronic system comprising:

a plurality of circuit modules includes a plurality of dies, wherein at least one die includes at least one array of memory cells, wherein the array comprises at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer;

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer;

a plurality of leads coupled to the plurality of dies to provide unilateral or bilateral communication and control; and

a user interface.

53. A computer system comprising:

a processor;

a memory system that comprises a plurality of memory modules, wherein one of the plurality of memory modules comprises a plurality of memory devices, wherein at least one memory device comprises at least one array of memory cells, wherein the array comprises at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired

diffusion of at least one substance of the first compound from the insulator layer; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer;

a plurality of command links coupled to the plurality of memory devices to communicate at least one command signal;

a plurality of data links coupled to the plurality of memory devices to communicate data;

a memory controller;

at least one user interface device, wherein the at least one user interface device includes a monitor;

at least one output device, wherein the at least one output device includes a printer; and

at least one bulk storage device.